

UNITED STATES PATENT AND TRADEMARK OFFICE  
**CERTIFICATE OF CORRECTION**

PATENT NO. : 6,794,711 B2  
DATED : September 21, 2004  
INVENTOR(S) : Kang et al.

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Column 4,

Line 36, "the select transistor" should read -- the select transistor II. --.

Column 5,

Line 56, "transistor II. The" should read -- transistor III. The --.

Column 6,

Line 43, "transistor m. At" should read -- transistor III. At --.

Column 7,

Line 12, "transistor m is" should read -- transistor III is --.

Line 23, "transistor m. Therefore," should read -- transistor III. Therefore, --.

Line 33, "transistor m. Their" should read -- transistor III. Their --.

Line 60, "transistor m is" should read -- transistor III is --.

Column 18,

Line 43, "among sidewall, of" should read -- among sidewalls of --.

Line 46, "gate structure an the" should read -- gate structure on the --.

Signed and Sealed this

Twelfth Day of July, 2005

A handwritten signature in black ink, appearing to read "Jon W. Dudas". The signature is stylized with a large, looped initial "J" and a cursive "Dudas".

JON W. DUDAS  
*Director of the United States Patent and Trademark Office*